**Lab 7**

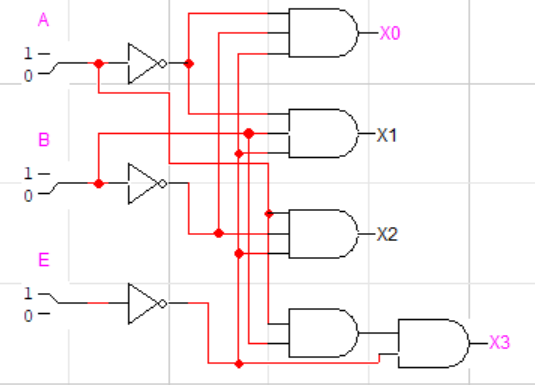
# Question 1:

**Make a truth table and implement 2x4 Decoder with a low enable using 8 AND gates and 3 NOT gates.**

**Truth Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **E** | **A** | **B** | **D0** | **D1** | **D2** | **D3** |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |

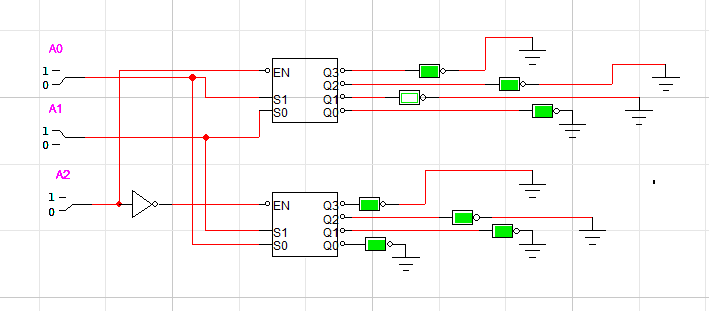
**Logic Works Implementation:**



# Question 2:

**Implement 3x8 decoder using two 2x4 decoders and NOT gate**

**Logic Works Implementation:**



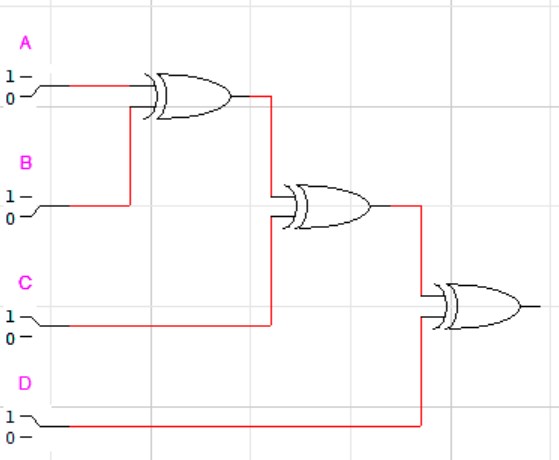
# Question 3:

**4 bit parity Checker**

**Implement a circuit that receives 4-bit message and outputs Error (E=1) if its parity is ODD**

**(Implement it using XOR and XNOR gates)**

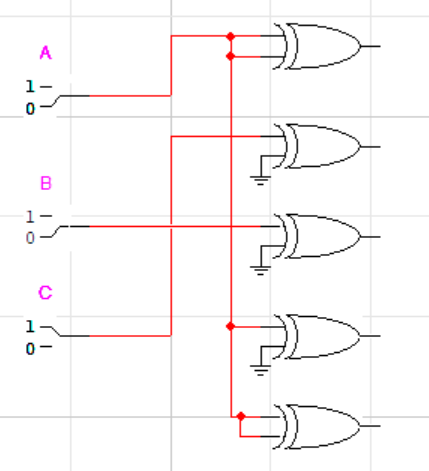
**Logic Works Implementation:**



# Question 4:

**Implement a doubler circuit. It takes a 3-bit input and multiplies it by two and gives a 5-bit output.**

**(Implement it using XOR and XNOR gates)**



**S0 = 0**

**S1 = C**

**S2 = B**

**S3 = A**

**S4 = 0**